Sept 2014	PHOENX JUMPER SETTINGS - ENGLISH	a1k.org

Jumper	Default position		Location	Function	Comments
JP2			Right of memory	Internal Power Connector 1 (4 pin)	
JP3			Right of memory	Internal Power Connector 2 (4 pin)	
JP4			bottom left	External SCSI Connector (26 pin)	
JP6			bottom left	Internal SCSI Connector (50 pin)	
JP7			right of zorro	Internal Floppy Connector 1 (34 pin)	
JP8	xxxx |||| xxxx xxxx	top closed	right of zorro	Drive Swap Switch see the Manual	by default, all should be closed
JP9			left and above zorro	internal serial	
L1	x-x	closed	left of main 28Mhz xtal	This is a 2-pin link that interrupts the 28Mhz feed to Agnus. This will normally be in, but will be taken out for a Super Obese Agnus. This because it is necessary to mix the XCLK signal before it is fed into the S.O. Agnus.	
L2	x-x	closed	right next to agnus	This is a 2-pin link that will normally be in, and must be for a Genlock to work. This link will probably be used with a S.O. Agnus	
L3	x x	open		back and right of U51	
L4	x-x x	left	above agnus	This is a 3-pin link that selects Fat or Obese Agnus mode on an Obese Agnus. In Fat Agnus mode, join 1&2 to get A23 onto pin 59 of Agnus. In Obese Agnus mode, join 2&3 to get A19 onto pin 59. Pins 1,2 and 3 are numbered left to right.	works in tandem with L55 and L56, see manual for configuration combinations
	x x-x	right			
	x x x	open			
L5	x x	open	3/4 up on J1	Activates pins 73 and 74 of 96-pin expansion connector (future use). (Pin 1 is at the bottom.)	
L6	x x	open	3/4 up on J1	Activates pins 71 and 72 of 96-pin expansion connector (future use). (Pin 1 is at the bottom.)	
L7	x x	open	3/4 up on J1	Activates pins 70 and 65 of 96-pin expansion connector (future use). (Pin 1 is at the bottom.)	
L8	x x	open	3/4 up on J1	Activates pins 66 and 67 of the 96-pin expansion connector (future use). (Pin 1 is at the bottom.)	
L9	x x	open	top left corner of EC2	This link feeds a buffered *CCK signal onto pin 19 of EC2 (the first B2000 video slot connector). This is not used at the moment.	
L10	x-x	closed	below Agnus	bootup in NTSC (28,636 Mhz)	
	x x	open		bootup in PAL (28,37516 Mhz)	
L11	x x-x	right	below Agnus	2MB Agnus installed	
	x-x x	left		1MB Agnus installed	

NOTE	In addition to jumper settings here, a custom PAL 70 must be installed for for Zorro capabilities!				
L12	**x-x**	closed	bottom left, next to LED connector	Autoconfig chain closed (active)	This jumper starts the auto-config chain; if it is removed, nothing will auto-configure (Front slot, onboard SCSI, Zorro slot, CPU Header and expansion bus)
	x x	open		Complete shutdown of the autoconfig chain	
L13	**x-x**	closed	bottom left, next to LED connector	Autoconfig chain closed (active)	Onboard SCSI, Zorro slot, CPU Header and expansion bus are completely removed from the Config-chain!
	x x	open		Autoconfig chain is interrupted (by front slot, before SCSI, Zorro, CPU and expansion port)	
L14	**x-x**	closed	between SCSI and RAM banks	Autoconfig chain closed (active)	Zorro slot, CPU Header and expanion bus are completely removed from the config-chain!
	x x	open		Autoconfig chain is interrupted (by front slot and SCSI before Zorro, CPU and expansion port)	
L15	**x-x**	closed	next to math coprocessor socket	Autoconfig chain closed (active)	Some docs have this listed incorrectly!
	x x	open		Autoconfig chain is interrupted (by front slot, SCSI and Zorro before CPU and expansion port)	CPU-Header and expansion bus are completely removed from the Config-chain!
L16	**x-x**	closed	below the 68000 socket	Bypasses the Phoenix custom CPU slot	No card in the CPU slot (68000 installed)
	x x	open		Activets the Phoenix custom CPU slot	Phoenix-Turbo card installed, 68000 removed
L17	x-x	closed	BL of external 86-pin expansion slot	Enables connection to the currently unused pin 11 of the 86-pin side expansion slot.	
	x x	open			
L18	**x-x**	closed	just right of the Zorro slot	This link hooks the BRN signal on pin 60 of the B2000 slot to the BUS REQUEST signal. This should normally be in.	Must always be closed!
	x x	open			
L19	**x-x**	closed	just right of the Zorro slot	This link hooks the BGN signal on pin 64 of the B2000 slot to the BG signal. This should normally be in.	Must always be closed!
	x x	open			
L20	**x x**	open	upper left of zorro slot	This provides connection to the unused pin 9 (NSLN) of the B2000 slot. This is not used at the moment.	
L21	**x x**	open	upper left of zorro slot	This provides connection to the unused pin 7 of the B2000 slot. This is not used at the moment.	
L22	**x x**	open	top end of zorro slot	This provides connection to the unused pin 98 of the B2000 slot. This is not used at the moment.	
L23	**x x**	open	top end of zorro slot	This provides connection to the unused pin 97 of the B2000 slot. This is not used at the moment.	
L24	**x x**	open	top end of zorro slot	This provides connection to the unused pin 93 (DOE) of the B2000 slot. This is not used at the moment.	

L25	**x** **|** **x** x	top closed	back of CN1	This 3-pin jumper controls the switching of the 7.5MHz audio filter. To allow software switching of the filter, pins 1&2 must be connected (this is the normal configuration). To disable the filter, pins 2&3 should be connected. If no pins are connected, the filter will be on. Therefore, if pins 2&3 are connected to a switch, the filter can be hardware switched.	
L26	**x** **x**	open	left of U61	This 2-pin jumper forms the left end of a 6-pin jumper block. It feeds into pins 18 and 19 of unused the 20L8 PAL U61 that controls the math coprocessor. It is not used at the moment.	
L27	**x** **x**	open	left of U61	This 2-pin jumper forms the right end of a 6-pin jumper block. It links pin 14 of the 20L8 PAL U61 to ground.	
L28	**x** **|** **x**	closed	left of U61	This 2-pin jumper forms the middle of a 6-pin jumper block. It feeds the DTACK signal from Gary to the 68000, and should be in if there is no math coprocessor present. If it is out, DTACK is not passed through, and the 20L8 PAL controlling the math coprocessor has to mix the DTACK signal from Gary with the DSACK from the math coprocessor, to produce a DTACK signal from the 68000.	
L29			top right of 74HC00	This is connected to the power LED, and is polarised. The topmost pin is positive.	
L30	**x x**	open	bottom right of 74HC01	This enables the connection of the interrupt from the SCSI chip to INT2 in Paula. This link should be left out for Phoenix's SCSI software.	

NOTICE	These jumpers provide configuration of the SCSI EPROM U31, so the EPROM can be used to auto-configure other devices, provide more information, and so a bigger EPROM than the current 27C64 can be used.				
L31	**x** **|** **x** x	top closed	right of SCSI Eprom U31 (bottom left of the board)	This provides A16 to pin 3 of the EPROM, or 5v to pin 3 of a smaller EPROM. Pins 1 & 2 must be joined for the SCSI to work reliably with the current 27C64.	
	x **x** **|** **x**	bottom closed			
L32	x | x x	top closed	right of SCSI Eprom U31 (bottom left of the board)	This provides A18 or ground to pin 30 of the EPROM. Pins 1&2 must be joined if a 27C64 is in use.	
	x **x** **|** **x**	bottom closed			
L33	**x-x** x	left	under SCSI Eprom U31 (bottom left of the board)	This provides A19 or power to pin 31 of the EPROM. This is not needed on a small EPROM.	
	x **x-x**	right			
	x x x	open			

L35	**x-x** x	left	under SCSI Eprom U31 (bottom left of the board)	SCSI-autoboot disabled	Buddha (front slot) should be stable; (A14 of the EPROM placed on A15) Note: With L35 is not the hardware of the Phoenix SCSI off but only the Integration of the pbscsi.device Suppressed or released startup
	x **x-x**	right		SCSI-autoboot enabled	e.g. ideal to of built-in SCSI HD boot and the Buddha an IDE CD drive join => if necessary but problems! (A14 down from the EPROM to VCC); U17 / U70 must be installed
	x x x	open		do not use	
L36	**x x**	open	bottom right of 5380 SCSI chip	This brings out the RDY, *EOP and DREP functions from the 5380, and pin 26 of the 26-pin SCSI expansion connector JP4.	
L37	x-x	closed	left of SCSI PAL U27	This is a 4-pin jumper block that is used to feed 2 additional inputs into the SCSI PAL, should these ever be used (they are not at the moment). 2 pins are ground the other 2 go to pins 1 and 11 of the SCSI PAL.	
	x x	open			
L38	**x x**	open	bottom of U54	This single pin jumper supplies the interrupt pulse from the RTC chip. It is not used at the moment.	
L39	**x x**	open	Left of keyboard connector	This 4-pin square jumper block is used if you are fitting an 8-way keyboard connector (as found on an A500 keyboard) instead of a 4-way connector. The 4 pins supply the power LED, the hardware reset line, the drive in-use LED and a blank pin. Wiring to these pins will be the responsibility of the end user.	
L40	x **x** **|** **x**	bottom closed	front right corner	This 3-pin jumper is used to feed the light pen signal that goes into Agnus from the fire button on either gameport 1 or gameport 2. On an A1000, light pens are connected to port 1 (this is the normal configuration on the Phoenix board), and to port 2 on an A500. Pins 1&2 must be connected for port 2, and pins 2&3 for port 1.	
L41	x **x-x**	right	top right of U58	This 3-pin jumper forms the bottom 3-pin row of a 6-pin jumper block. Pin 1 is to the left, and is connected to A18. Pin 2 is connected to pin 30 of the EPROMs, and pin 3 is connected to power. If using the original Kickstart-in-ROM EPROMs, 2&3 must be joined to supply power for these smaller 28-pin EPROMs. If using larger EPROMs, 1&2 must be joined to supply A18.	

L42	x x		under Agnus, above ROM socket #4	These two jumpers combine to select one of the 4 Kickstart ROM sockets (see manual). These jumpers are normally used together with a switch.	L42 = lowest four pins of a 20 pin vertical jumper block. Note that if you have the onboard SCSI, you must set L35 to the left if you ever want to disable SCSI autoboot.
	x x				
L43	**x-x**	closed	left of memory bank	Ground all DRAMs when closed	Must always be closed!
L44	**x-x**	closed	left of U53	This 2-pin jumper connects the chip enable of U53 (pin 1 of the jumper to ground (pin 2). This jumper must be in to enable U53, which is the first and standard Kickstart ROM.	
L45	**x-x**	closed	top left of U53	This 2-pin jumper controls U54, the second Kickstart ROM. It is normally out. If U53 and U54 were both to be used (for a Kickstart swap switch for instance), L44 and L45 would have to be switched.	
L46	**x-x**	closed	next to main xtal	This 2-pin jumper is part of a 4-pin jumper block (the other 2-pin jumper being L60). L46 is the top two pins. This jumper connects ground to pin 22 (chip enable) of all the 8-bit Kickstart EPROM sockets, and is used to enable Kickstart in these sockets.	
L47, L48	**x x**	open	Top left of U60	L47 and L48 are the first four pins of a 7-pin jumper strip (the last three pins is L56). L47 and L48 bypass the CAS upper and CAS lower (with L47 controlling the lower) signals around U60 (the PAL controlling 2 megabytes of onboard RAM). For only 1 megabyte of RAM on the motherboard, both these jumpers must be open.	Default is open for a 1MB Agnus, both should be closed for a 2MB Agnus
	x x	open			
L49, L50, L51, L52	**x x**	open	bototm left of U51, near Agnus	These jumpers feed into spare inputs of the 74HC541 buffer chip, and are not used at the moment.	
L53	**x x**	open	top left of U61	This jumper selects chip enable for the 16 bit Kickstart EPROM U61, and should be out unless a Kickstart ROM is intalled there.	
L54	**x x x**	open	top of U60	Pin 3 (to the left) of this 3-pin jumper is connected to ground and pin 1 is connected to L81 which is immediately above it. Pin 2 is connected to pin 10 of U60 (a 20L10 PAL). This allows ground or another signal from L81 to be fed into U60, so that a smaller 20-pin chip could be plugged into U60. This is not implemented or used at the moment.	
L55	xxx xxx	left	left of ROM socket #4	Memory Configuration => see the storage table (and L4, L56!)	memory starts at $100000 (for RAM conflicts like AMax)
		right			memory starts at $C00000 (amiga default)
		open			open for 2MB Agnus

L56	**x-x** x	left	left of ROM socket #4	Memory Configuration => see the storage table (and L4, L56!)	default is left
	x x-x	right			
	x x x	open			open for 2MB Agnus
L57	**x x x**	open	top left of U58	This 3-pin jumper is the bottom row of a 6-pin jumper block (the top row is L58). Pin 2 connects to pin 29 of the four 32-pin Kickstart EPROM sockets. Pin 1 provides A15, to enable the use of larger EPROMs. Pin 3 provides the C25 read/write signal from the processor. With pin 3 connected, the EPROMs can be replaced with static RAM, which could be battery backed with a simple board mod. This link is normally out for CBM Kickstart ROMs.	
L58	x **x-x**	left	top left of U58	This 3-pin jumper is the top row of a 6-pin umper block (the bottom row is L57). Pin 2 goes to pin 3 of the 32-pin EPROM sockets. Pin 1 provides A15, and pin 3 provides A16.	
L59	**x x x**	open	right of U58	This 3-pin jumper is the top row of a 6-pin jumper block. It puts either A19 or A16 onto pin 31 of the 32-pin EPROMs. It is normally out for Kickstart ROMs.	
L60	**x x**	open	bottom right of xtal	This 2-pin jumper is part of a 4-pin jumper block, and enables the ROMEN signal from pin 2 of the controlling PAL to bypass the PAL and join to pin 13 (the output enable line of U53). This link must be in if the PAL U59 is present, and vice versa.	
L61	**x x**	open	right of J1	This jumper connects to pins 75 and 76 of the 96-pin expansion connector, J1. It is not used at the moment.	
L62, L63			top of 68000	These pins connect to pins 8,9 and 10 of resistor pack RP3. Pin 10 of that pack (L64) is now used to pull-up pin 5 of U15, but pins 8 and 9 are unused.	
L64	**x-x**	closed	bottom left, next to LED connector	Bridging configuration lines front slot	If no extension inserted in front slot this Jumper must be closed (includes the Autoconfigkette)
	x x	open		Activation front slot	Open only if an Autoconfig expansion is in the front slot, otherwise the entire config Chain is shut down - even the onboard Phoenix SCSI!
L65	x x	open	below RP4	This jumper connects to pin 9 of the 470ohm resistor pack RP4, and can be usedas a pull-up resistor.	

L66	x	open		This 1-pin link is not on the circuit diagrams at the moment. It connects to the unused pin 20 of the B2000 connector.	
L67, L68, L69, L70, L71		unused	left of Paula	These 5 1-pin links are connected to the unused bottom 5 pins of resistor pack RP1, to provide pull-up resistors.	
L72, L73, L74		unused	top of EC2	These three 1-pin links connect to the unused pins 1, 5 and 2 (respectively) of EC2, the first B2000 video socket.	
L75, L76		unused	bottom of EC2	These two 1-pin links connect to the unused pins 36 and 35 of EC2	
L77, L78, L79, L80		unused	right of U51	These links are the middle 8 pins of a large link block to the right of U51, and connect the pins 14, 13, 12 and 11 (respectively) of U51 (the 74HC541 buffer).	
L81		unused	top of U60	See description for L54	
L82, L83, L84, L85, L86, L87, L88, L89, L90, L91, L92, L93, L94, L95, L96			near internal and external RS232 sockets	These 15 1-pin links provide connections to spare pins on both the internal and external RS232 sockets. P5 is the external RS232 socket, JP9 is the internal one. The connections are as follows: L82 -> 19 of P5, L83 -> 9 of P5, L84 -> 10 of P5, L85 -> 11 of P5 L86 -> 12 of P5, L87 -> 13 of P5, L88 -> 22 of P5, L89 -> 26 of P5 L90 -> 18 of JP9, L91 -> 12 of JP9, L92 -> 17 of JP9, L93 -> 23 of JP9 L94 -> 19 of JP9, L95 -> 21 of JP9, L96 -> 25 of JP9	
L97			near P4	This 1-pin link connects to pin 24 of P4 (the parallel connector)	
L98			left of U63	This 1-pin link connects to the only unused pin on the CIA U63, pin 18.	
L99, L100, L102, L102		unused	under U56	These 1-pin links connect to pins 2,5,9 and 12 of the 1489 RS232 receiver U65, and are used to modify certain characteristics of RS232 operation. These are not used at the moment.	
L103	**x-x**	closed	next to 68000	This jumper joins the main clock pin of the 68000, pin 15, to pin 38, the 7MHz output of Agnus. Pin 1 of the jumper (on the right) goes to pin 15 on the 68000, and pin 2 goes via R1 to pin 38 of Agnus. This jumper is normally in, but can be removed and used in conjunction with a 74F74 to perform "processor speed-up" hacks.	
L104				This 1-pin link is connected to the 28MHz clock signal, after it has passed through a ferrite bead.	
L105, L106, L107	**x-x**	closed	right of U51	These jumpers will all perform different functions with a 2MB Agnus, but with an 1MB Agnus must all be in.	

L108, L109, L110, L111			near U69	These jumpers are found under and around the spare 14-pin socket, U69, and connect to various pins of that socket	
L112, L113, L114, L115, L116			right above Zorro	These links are found around the spare 20-pin socket, U68, and connect to various pins of that socket.	
L117	**x x** **x x** **x x**	closed	upper right of Zorro	These jumpers must be closed if the U70 IPL PAL is not used. This chip is only used if the B2000 socket is fitted, to combine interrupts from the B2000 slot and pass them to inputs of the 68000.	When autoconfig installed Zorro card: all should be open!
L118	**x-x**	closed	near U70	Similar to above.	Keep open if U70 is present
L119	**x-x** **x-x**	closed	around SCSI Eprom U31 (bottom left of the board)	If the 2 megabyte controlling PAL U60 is not installed, this jumper must be in, to convey A23 back to A19 on Gary. This jumper is a square 4-pin link, and is the second 4 pins of an 18-pin link block.	all 4 jumper blocks should be closed
L120	x-x	closed	under storage	Does not activate the onboard SCSI controller	allways keep this open!
	x x	open		Activate SCSI controller	
L121	x-x	closed	under Agnus, left of Zorro, silkscreen covered by cap c100	skips Zorro slot	Set if no card in zorro slot
	x x	open		Activate Zorro slot	Set is there is a card in the Zorro slot
L122	**x-x**	closed	Near CPU	AutoConfig chain bridged (active) to the expansion port	With expansion port extension installed
	x x	open		Separates config chain to the expansion port	
L123			left edge of board past JP4	This brings out pins 25 and 34 of the 50-pin SCSI connector, should they ever need to be used (they are not at the moment).	
L124				This pin is on the lead from pin 13 of the parallel port to pin 4 of the CIA U63, and may be used if a mod is done to have an RI signal on the serial port, as is the case in the A500.	
L125	x-x x	left	right of U64	time&date set from 50hz main tick (PSU)	
	x x-x	right		time&date set from 50hz vertical sync	
L126	**x-x**	closed	left rear		
L130, L131			near JP10	These two 1-pin links connect to pins 1 and 6 of the (often) unused 8-pin DIN connector JP10 at the back of the board.	
L132	**x x** **|** **x x**	right	left of U60	If the 2 megabyte controlling PAL U60 is not installed, pins 3 and 4 must be joined. If it is installed, pins 1 and 3 must be joined. This link is a square 4-pin link, and is the top 4 pins of an 18-pin link block.	keep set to right
L133	**x-x**	closed	left of memory bank	controlls 1x4 or 256x4 drams	out for 2mb Agnus (1mx4 DIP DRAM)
R88	**x-x**	closed	left rear		
R42	**x-x**	closed	left rear		